

FEATURES

- Femtosecond integrated phase jitter
- Superior phase noise
- Miniature package sized available

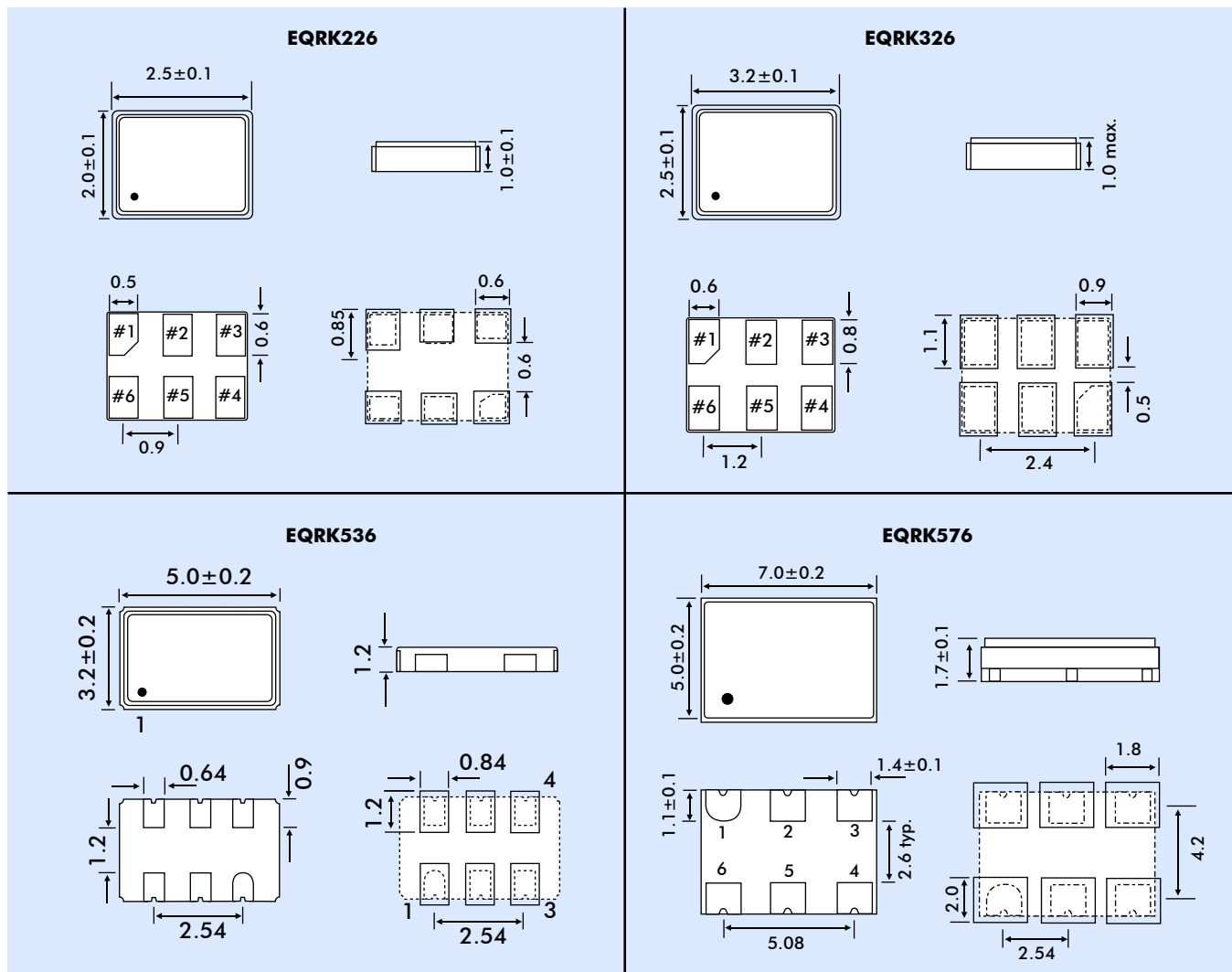

GENERAL SPECIFICATIONS at $T_a = +25^{\circ}\text{C}$

Output Logic	LVPECL	LVDS		HCSL	
Supply Voltage	--	--	1.8V $\pm$ 5%	--	+1.8 Vdd $\pm$ 5%
	+2.5 Vdd $\pm$ 10%	+2.5 Vdd $\pm$ 10%	--	+2.5 Vdd $\pm$ 10%	--
	+3.3 Vdd $\pm$ 10%	+3.3 Vdd $\pm$ 10%	--	+3.3 Vdd $\pm$ 10%	--
Available Frequency Range	10~250MHz	10~250MHz	10~160MHz 180 ~ 250MHz	20 ~ 50MHz 60 ~ 220MHz	100 ~ 160MHz
Load	50 Ω into Vdd -2V or Thevenin equivalent	100 Ω between output and complementary output		50 Ω to GND on both outputs	
Output Logic 'HIGH' '1'	Vdd - 1.03 min. Vdd - 0.6 max.	1.4V typ. 1.6V max.	0.8V typ. 1.0V max.	550mV min. 1.0V max.	
Output Logic 'LOW' '0'	Vdd - 1.85 min. Vdd - 1.6 max.	0.9V min. 1.1V typ.	0.3V min. 0.5V typ.	-150mV min. 150mV max.	
Current Consumption (Vdd = +3.3V)	32mA typ. 60mA max.	10mA typ. 25mA max.	8mA typ. 16mA max.	17mA typ. 35mA max.	
Output Voltage Swing	500mV min. 750mV typ.	300mV min. 400mV typ. 480mV max.	200mV min. 300mV typ. 400mV max.	500mV min.	
Rise/Fall Time	5ns max. (20%~80% wavef.)	0.35ns max. (20%~80% wavef.)	0.35ns max. (20%~80% wavef.)	0.35ns max. (20%~80% wavef.)	

Phase Jitter, rms (typical) (12kHz to 20MHz)	84fsec typ.; For 156.250MHz, LVPECL 3.3V						
Frequency Stability Codes	Frequency Stability over Operating Temp. Range	±25ppm		±50ppm		±100ppm	
	Commercial (-10° to +70°C)	A		B		C	
	Industrial (-40° to +85°C)	D		E		F	
	Extended Industrial (-40°C to +105°C)	G		H		I	
Duty Cycle	50%±5%						
Start-up Time	0.75ms typical, 2.0ms maximum						
Ageing at 25°C	±3ppm maximum for first year; ±2ppm (max) per year thereafter						
Storage Temp. Range	-55° to +150°C						
OUTPUT ENABLE FUNCTION							
OE Control on pin 1	70% of Vdd (min.) To enable Output						
	30% of Vdd (max.) To disable output						
Output Enable Time	2.0ms max.						
Output Disable Time	0.2μs max.						
SSB Phase Noise [dBc/Hz typ.]	Offset	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz
	156.250MHz	-63	-97	-134	-139	-148	-153

Package Drawings & Ordering Information Overleaf

OUTLINE DIMENSIONS (Unit: mm) SUGGESTED PAD LAYOUT FOR SMDs



Pad Connections

- Pad 1: OE or No Connection
- Pad 2: OE or No Connection
- Pad 3: Ground
- Pad 4: Output
- Pad 5: Complementary Output
- Pad 6: Supply Voltage

PART NUMBER FORMAT AND EXAMPLE

Example: 25 EQDRK 226 1 - E - 120.000

Supply Voltage

- 18 = 1.8 Volts
- 25 = 2.5 Volts
- 3 = 3.3 Volts

Output Type

- P = LVPECL
- D = LVDS
- C = HCSL

Package

- 576 = 7.0 x 5.0mm
- 536 = 5.0 x 3.2mm
- 326 = 3.2 x 2.5mm
- 226 = 2.5 x 2.0mm

Output Enable

- 1 = OE on pin 1
- 2 = OE on pin 2

Frequency Stability

Frequency in MHz

Issue 1