

HPK3261 PECL OSCILLATORS

3.2 x 2.5 x 1.0mm 6 pad SMD

13.50MHz to 220.0MHz

DESCRIPTION

- Femtosecond integrated phase jitter (200fs typical)
- Ultra-low phase noise -138dBc/Hz at 10kHz
- · High performance with surprisingly low price
- Supply voltage 2.5 or 3.3 Volts





SPECIFICATION

Frequency Panae:

	rrequency kange:	13.3MMZ 10 ZZU.UMMZ		
	Output Logic	Differential PECL square wave		
	Phase Noise:	See table		
	Frequency Stability:	See table		
	Operating Temp Range			
	Commercial:	-10° to +70°C		
	Industrial:	-40° to +85°C		
	Input Voltage:	+2.5V ±5% or +3.3VDC ±10%		
	Output Voltage			
	HIGH '1':	Vdd - 1.03V min., Vdd - 0.6V max.		
	LOW '0':	Vdd - 1.85V min., Vdd - 1.6V max.		
		$(RL = 50\Omega \text{ to Vcc -2.0V})$		
	Output Swing:	595mV min., 750mV typ., 930mV max		
	Load:	50Ω into Vcc-2V or Thevenin		
		equivalent. Terminating resistors		
		required on all outputs.		
	Rise/Fall Times:	2.5V: 0.3nsec typ., 0.6nsec max.		
		3.3V: 0.2nsec typ., 0.4nsec max.		
	Duty Cycle:	50±5% (measured at 50% waveform)		
	Current Consumption:	30mA typical, 50mA maximum		
	Start-up Time:	5ms typ., 10ms max.		
	Integrated Phase Jitter:	0.2ps typical; 0.5ps maximum		
		for 156.250MHz (12kHz to 20MHz)		
	Ageing:	±3ppm per year max., ±2ppm		
		thereafter. At T amb +25°C		
	Packaging:	16mm tape, 8.0mm pitch. 180mm		
		dia. reel, 1000 pieces per reel.		

13 5MHz to 220 0MHz

ENABLE/DISABLE (TRISTATE) FUNCTION

The Enable/Disable function may be on Pad 1 or Pad 2

HPK3261 = Enable/Disable control on Pad 1 HPK3262 = Enable/Disable control on Pad 2

NO CONNECTION	Differential and Complimentary outputs enabled.
DISABLE	Both outputs are disabled (high impedance) when Control Pad is taken below 0.45*Vcc referenced to Ground (threshold). Oscillator is always ON. Only the buffer stage is disabled.
ENABLE	Both outputs are enabled when Control Pad is taken above 0.45*Vcc referenced to Ground (threshold). Enable time 10ns +1 period of output frequency maximum.

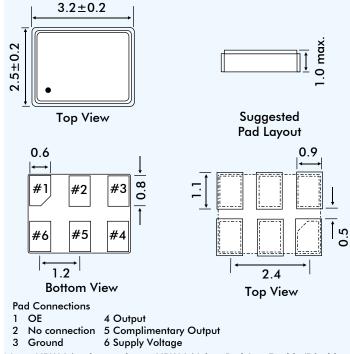
TYPICAL PHASE NOISE (62.5MHz)

Offset	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz
dBc/Hz	-50	-82	-116	-138	-144	-149

TYPICAL PHASE NOISE (156.250MHz)

Offset	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz
dBc/Hz	-50	-80	-115	-135	-142	-147

OUTLINE & DIMENSIONS



Note: HPK3261 shown above; HPK3262 has Pad 2 = Enable/Disable and Pad 1 No Connection.

STABILITY OVER TEMPERATURE RANGE*

Stability ±ppm	Temperature Range °C	Order Code
25	-10 to +70	Α
50	-10 to +70	В
100	-10 to +70	С
25	-40 to +85	D
50	-40 to +85	E
100	-40 to +85	F

* Custom frequency stability is available; e.g. for +/-20 ppm over -10 to $+60^{\circ}$ C use 'C' for custom, I.e. C20.

Storage Temperature: -55°C to +150°C

PART NUMBERS

HPK5361 oscillator part numbers are derived as follows:

Example: 25HPK3261-A-155.520

