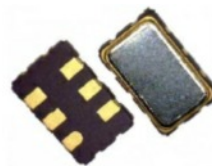


FEATURES

- Switchable Output Frequency Oscillators
- Outputs CMOS, LVPECL, LVDS,
- Hi Frequency Range - 10.000MHz to 1.5GHz
- Available in 7 x 5mm, 5 x 3.2mm & 3 x 2.5mm formats
- Short Lead Time, Quick Delivery
- RMS phase jitter 1.5ps typical
- ITAR Free


GENERAL SPECIFICATIONS

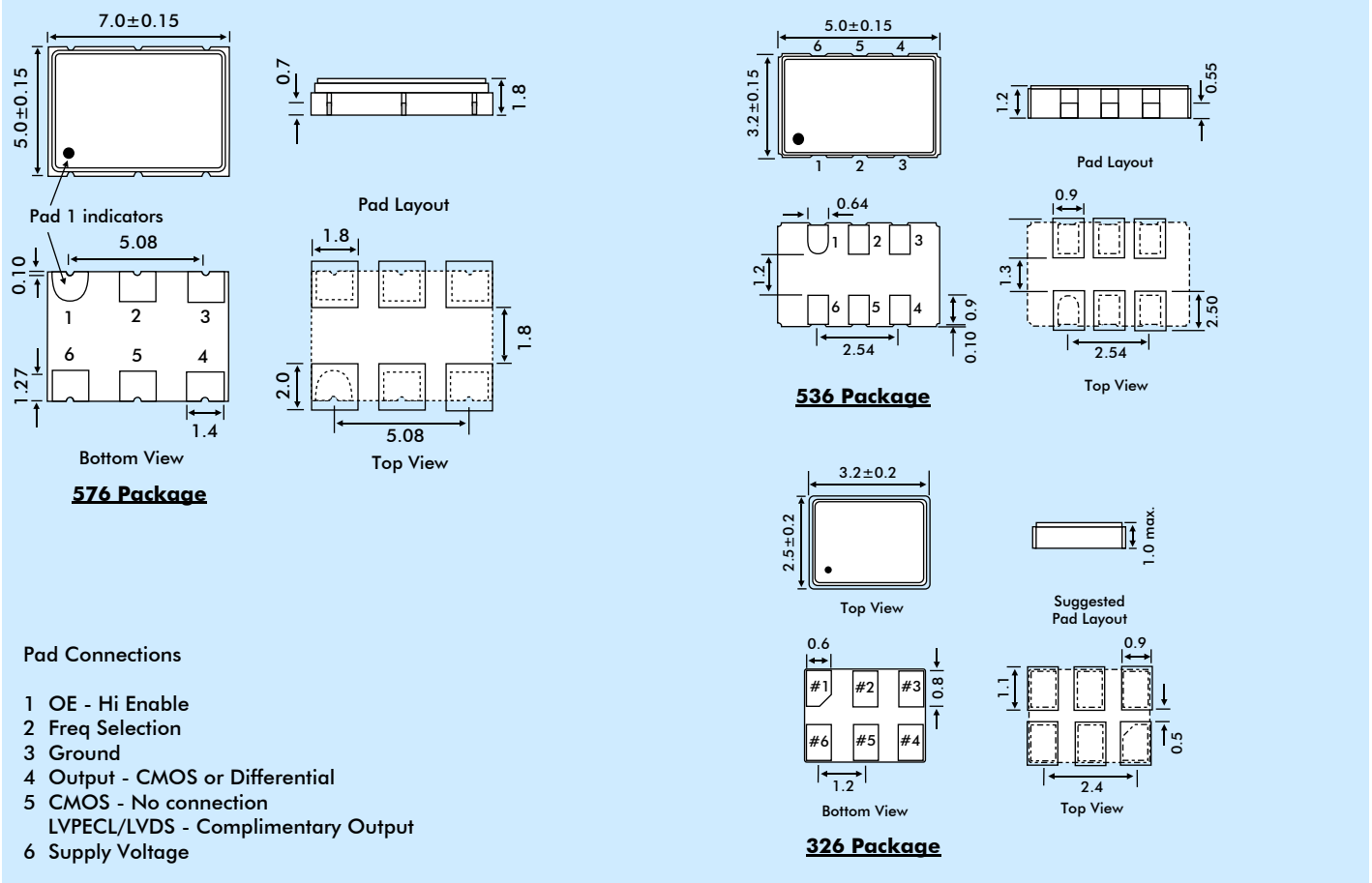
Output Logic Type	LVC MOS	LVPECL	LVDS
Frequency Range	10MHz ~250MHz	10MHz ~ 1500MHz	10MHz ~ 1500MHz
Load	15pF max	50Ω into V _{DD} -2V or Thevenin equivalent	100Ω between OUT and OUT-1
Power Supply Voltage (V _{DD})	+2.5V±5% or +3.3V±5%	+2.5V±5% or +3.3V±5%	+2.5V±5% or +3.3V±5%
Logic 'HIGH' Voltage	90% V _{DD}	V _{DD} -1.03 min, V _{DD} -0.6 max	1.4 V typ, 1.6V max
Logic 'LOW' Voltage	10% V _{DD}	V _{DD} -1.85 min V _{DD} -1.6 max	1.1V typical, 0.9V min
Duty Cycle	50%±5% 50%±10% 1.8V only	50%±5%	50%±5%
Rise Time (Tr) Fall Time (Tf)	10.0ns max. (10% ~ 90% waveform)	0.5ns max. (20% ~ 80% waveform)	0.4ns max. (20% ~ 80% waveform)
Current Consumption At V _{DD} = 2.5V	100MHz : 35mA 250MHz : 40mA	400MHz: 40mA 600MHz: 45mA 1GHz: 50mA 1.5GHz: 55mA	400MHz: 30mA 600MHz: 30mA 1GHz: 35mA 1.5GHz: 35mA
Current with output Disabled	18mA typical	18mA typical	18mA typical
RMS Phase Jitter (Typical) 12kHz to 20MHz	100MHz: 0.8ps 250MHz: 0.8ps	<400MHz: 0.8ps 600MHz: 1.0ps 1GHz: 1.3ps 1.5GHz: 1.7ps	<400MHz: 0.8ps 600MHz: 0.8ps 1GHz: 1.1ps 1.5GHz: 1.3ps
Output Enable/disable	70% V _{DD} min. pad 1 to enable ; 30% V _{DD} max. Pad 1 disable (open connection prohibit)		
Output Enable Time	200ns max enable, 50ns max disable		
Freq Selection (Pad 2)	FSEL= 0 then O/P Freq is first freq. (f1) FSEL= 1 then O/P Freq is second freq. (f2) Default FSEL pin has internal pull-up resistor		
Storage Temp	-55C +150C max limits		
Ageing at Ta = 25°C	±5ppm max. first year		

Frequency Stability Codes	Frequency stability over operating temp. Range	±25ppm	±50ppm	±100ppm	If non-standard please enter the desired stability after the 'C' or 'I' Example: 'C20' is ±20ppm over -10° to +70°C.
	Commercial -10° to +70°C	A	B	C	
	Industrial -40° to 85°C	D	E	F	

SSB PHASE NOISE DATA (@30.000MHz)

Offset	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz	5MHz	10MHz	20MHz
DBc/Hz	-66.59	-95.22	-114.27	-119.88	-122.93	-142.08	-148.14	-150.88	-154.63

OUTLINE & DIMENSIONS



PART NUMBERING

ECQF oscillator part numbers are configured as per the following example: ECQF-3-P-576-E-644.53

ECQF - 3 - P - 576 - E - 644.53

Series Code - ECQF

Supply Voltage
3 - 3.3V
25 - 2.5V
18 - 1.8V

Output Logic
T - CMOS
P - LVPECL
D - LVDS

Package
576 = 7 x 5mm
536 = 5 x 3.2mm
326 = 3 x 2.5mm

Stability & Operating Temp. Code
(See page 1)

Frequency (MHz)