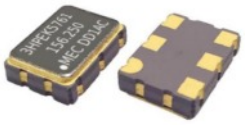
EUROQUARTZ

EK Series Differential Oscillators

'EH_EK' Low Phase Noise Oscillators 13.5MHz to 220MHz

FEATURES

- **LVPECL, LVDS, HCSL output available**
- **Femto second integrated phase jitter (98fs typical at 12KHz to 20MHz)**
- **Superior Phase Noise (-149 dBc/Hz at 100kHz and -157dBc/Hz at 10MHz offset)**
- **2.5x2.0mm, 3.2x2.5mm, 5.0x3.2mm, 7.0x5.0mm available**



RoHS REACH COMPLIANCE

General Specifications at Ta=+25˚C

Model	EHPEK	EHDEK	EHCEK
Output Logic	LVPECL	LVDS	HCSL
Available Frequency Range	13.5 MHz ~ 60MHz 90MHz ~ 220MHz	13.5 MHz ~ 60 MHz 90 MHz ~ 220 MHz	13.5 MHz ~60 MHz 90 MHz ~ 220 MHz
Supply Voltage	--	+2.5V ± 10%	+2.5V ± 10%
	+3.3V ±10%	+3.3V ± 10%	+3.3V ± 10%
Output Load - (V_{DD})	50Ω V_{DD} - 2.0V Or Thevenin equivalent	100Ω between output and complimentary output	50Ω to ground on each output
Rise Time / Fall Time (20%~80% of waveform)	0.2 nsec (typ.) 0.4 nsec (max.)	0.2 nsec (typ.) 0.4 nsec (max.)	0.5 nsec (typ.) 0.8 nsec (max.)
Current Consumption	38mA (typ.), 60mA (max.)	15mA (typ.), 35mA (max.)	32mA (typ.), 40mA (max.)
Output Logic "High", "1"	V_{DD} - 103 (min.),V_{DD} - 0.88(max.)	1.4V (typ.), 1.6V (max.)	0.5V (min.), 0.9V (max.)
Output Logic "Low", "0"	V_{DD} - 1.81 (min.),V_{DD} - 1.52(max.)	0.9V (min.), 1.1V (typ.)	-0.15V (min.), 0.15V (max.)
Output Swing (single-end)	400mV (min.)	250mV (min.)	500mV (min.)

Frequency Stability Codes	Frequency Stability over Operating Temperature Range	±25ppm	±50ppm	±100ppm	If non-standard, please ender desired stability after "C" or "I". For Example "C20" is +-20ppm over -10˚C to 80˚C "I30" is +-30ppm over -40˚C to 85˚C
	Commercial (-10˚C to +70˚C)	A	B	C	
	Industrial (-40˚C to +85˚C)	D	E	F	

Startup TIme	1.0 msec. (Typ.), 5.0 msec (max.)						
Duty Cycle	50% ±5%						
Storage Temperature	-55˚C to +150˚C						
Aging at Ta = 25C	±3ppm (max.) first year						
RMS Jitter (12kHz to 20MHz)	Freq. Output <100MHz: 350fs (typ.), [50Hz, 3.3V, LVDS]						
	Freq. Output >100MHz: 98fsec (typ.), [156.250MHz, 3.3V, LVDS]						
Phase Noise]DBc/Hz (typ.)]	Offset	100Hz	1kHz	10kHz	100kHz	1MHz	10MHz
	50MHz	-104	-134	-147	-153	-152	-157
	156.250MHz	-93	-123	-140	-149	-152	-157
Output Enable/Disable Function	Enable	70% (min.) of V_{DD} to enable output Enable time: 5 msec (max.)					
	Disable	30% (max.) of V_{DD} to disable output Disable current: 10uA (max.) [OE<=0.3V], DIsable time: 0.2 usec (max.)					

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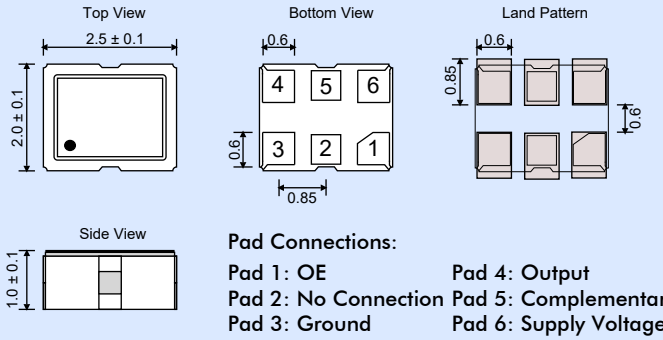
Outline DImensions (in mm), suggested pad layout, and test circuits

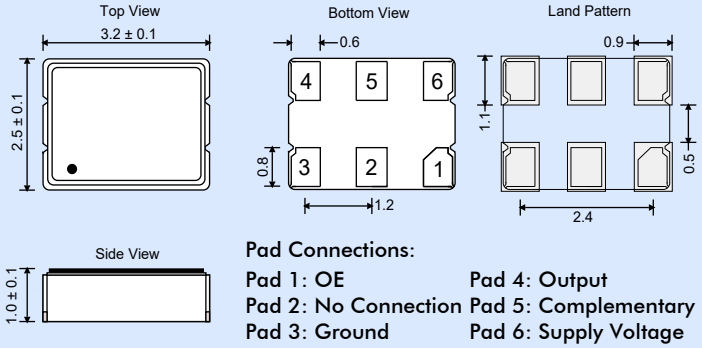
[EH__EK226]



Pad Connections:

Pad 1: OE
Pad 2: No Connection
Pad 3: Ground
Pad 4: Output
Pad 5: Complementary
Pad 6: Supply Voltage

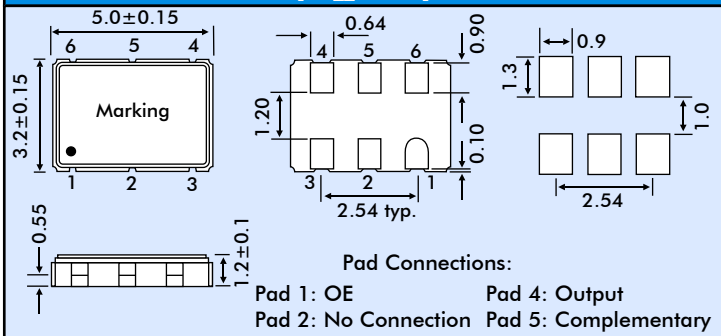
[EH__EK326]



Pad Connections:

Pad 1: OE
Pad 2: No Connection
Pad 3: Ground
Pad 4: Output
Pad 5: Complementary
Pad 6: Supply Voltage

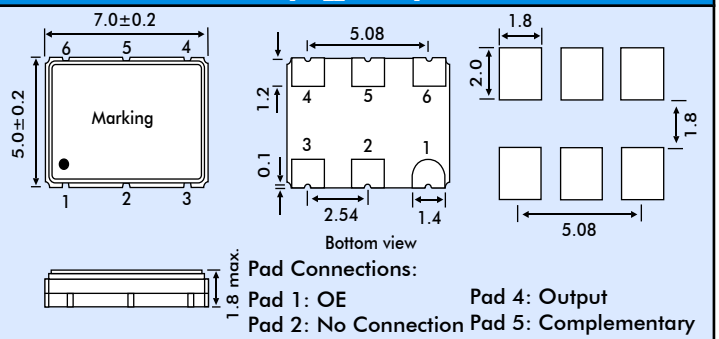
[EH__EK536]



Pad Connections:

Pad 1: OE
Pad 2: No Connection
Pad 3: Ground
Pad 4: Output
Pad 5: Complementary
Pad 6: Supply Voltage

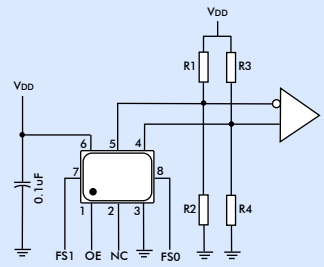
[EK__EH576]



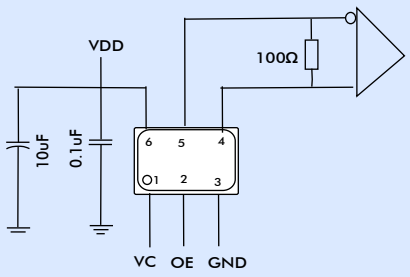
Pad Connections:

Pad 1: OE
Pad 2: No Connection
Pad 3: Ground
Pad 4: Output
Pad 5: Complementary
Pad 6: Supply Voltage

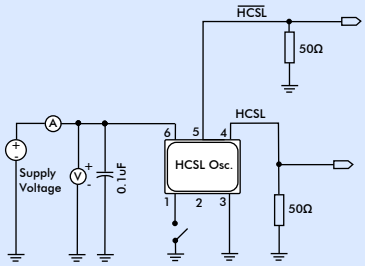
LVPECL Test Circuit



LVDS Test Circuit



HCSL Test Cicruit



Part Number Format

EH_EK part numbers are derived as follows:
Example: 125.000-25-EHCEK576-1-E

125.000 25 EHCEK576 1 E

Frequency

Supply Voltage:
25 = 2.5V
33 = 3.3V

Output
C = HCSL
D = LVDS
P = LVPECL

Package Size
226 = 2.5x2.0mm
326 = 3.2x2.5mm
536 = 5.0x3.2mm
576 = 7.0x5.0mm

OE function placement
1 = Pad 1
2 = Pad 2

Frequency Stablity Code
A~F (see stability table)

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