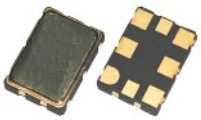
5 x 3.2 x 1.4mm Hi Freq Ultra Low Jitter Oscillator *15MHz - 1300MHz*

FEATURES

- **Wide frequency range 15MHz to 1300MHz**
- **Short lead time in both standard and custom frequencies**
- **Ultra low jitter 300fs rms**
- **Differential Output LVPECL, LVDS, HCSL and CML**
- **Available in a TCXO format**
- **Supply voltage options 1.8V, 2.5V or 3.3V DC**



DESCRIPTION

The EMVJF538 crystal oscillators are able to be delivered in days. The parts have gained their position in the frequency control market by the ability to deliver samples for prototypes at low cost quickly without compromise on performance.

GENERAL SPECIFICATIONS at Ta = +25°C

Model	EVMJF538P	EVMJF538D	EVMJF538C	EVMJF538Q
Output Logic	LVPECL	LVDS	HCSL	CML
Supply Voltage	-----	-----	+1.8 Vdd ±5%	+1.8 Vdd ±5%
	+2.5 Vdd ±10%	+2.5 Vdd ±10%	+2.5 Vdd ±10%	+2.5 Vdd ±10%
	+3.3 Vdd ±10%	+3.3 Vdd ±10%	+3.3 Vdd ±10%	+3.3 Vdd ±10%
Available Frequency Range	15~1300MHz	15~1300MHz	15~700MHz	150~1300MHz
Load	50Ω into Vdd -2V or Thevenin equivalent	100Ω between output/complimentary output	50Ω to GND	50Ω to Vdd
Output Logic 'HIGH' '1'	Vdd -1.03V min. Vdd - 0.6V max.	1.4V typ. 1.6V max.	Vdd: 0.66V min. Vdd: 1.15V max.	Vdd - 0.6V min. Vdd -0.32V max.
Output Logic 'LOW' '0'	Vdd -2.0V min. Vdd -1.55V max.	1.1V typ. 0.9V max.	Vdd: 0.0V min. Vdd: 0.15V max.	Vdd - 0.6V min. Vdd - 0.32V max.
Output Voltage Swing	595mV min 750mV typ 930mV max	250mV min 350mV typ 450mV max	620mV min 700mV typ 780mV max	200mV min 600mV typ
Current Consumption (Vdd = +3.3V)	100mA typ. 120mA max.	75mA typ. 90mA max.	80mA typ. 100mA max.	70mA typ. 85mA max.
Current with O/P Disabled	99mA typ.	74mA typ.	79mA typ.	69mA typ.
Rise/Fall Time	0.4ns max. (20%~80% wavef.)	0.4ns max. (20%~80% wavef.)	0.4ns max. (20%~80% wavef.)	0.4ns max. (20%~80% wavef.)

Phase Jitter, rms (typical) (12kHz to 20MHz)	15MHz~50MHz -500fsec : 51MHz -1,200MHz 250fs :				
Frequency Stability Codes	Frequency Stability over Operating Temp. Range	±25ppm	±50ppm	±100ppm	
	Commercial *(-10° to +70°C)*	*A*	*B*	C	
	Industrial *(-40° to +85°C)*	*D*	*E*	*F*	
Duty Cycle	50%±5%				
Start-up Time	5ms typical, 10ms maximum				
Ageing at 25°C	±3ppm maximum for first year; ±2ppm (max) per year thereafter				
Storage Temp. Range	-55° to +150°C				

Control Voltage Function on pad 1	**Output Enable Function on pad 2**	
+1.5V±1V for both V_{DD}= 2.5V and 3.3V	Output Enable	70% of VDD (min) to enable output
+0.9V±0.6V for both V_{DD}= 2.5V and 3.3V	Output Disable	30% of VDD (max) to disable output

Frequency Pulling Range	±8ppm min	
Linearity	±1% (typ) ±10% (max)	
Transfer Function	Positive Transfer	
O/P Enable/Disable Time	2.5msec max (enable) 10µs max.(Disable)	

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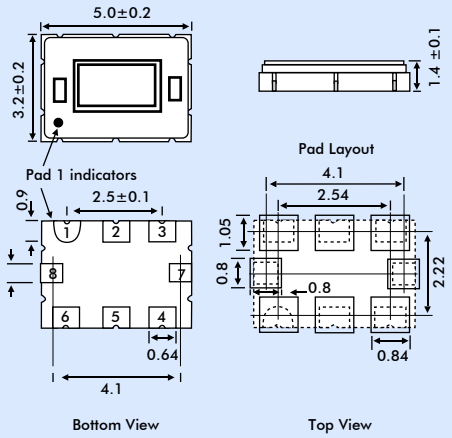
OUTLINE DIMENSIONS (Unit: mm) **SUGGESTED PAD LAYOUT FOR SMDs**



PAD CONNECTION
Pad1: VCTCXO: CTL voltage
TCXO: Ground
Pad2: OE
Pad3: Ground
Pad4: Output
Pad5: Complimentary output
Pad6: Supply Voltage
Pad7: Do not connect
Pad8: Do not connect

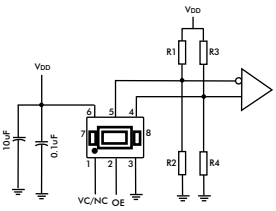
PART NUMBER FORMAT AND EXAMPLE

EXAMPLE: 3EVMJF538 - P - 156.250MHz-

33	EVMJF	538	/	P	/	156.25 MHz
Supply Voltage '33' for 3.3V '25' for 2.5V '18' for 1.8V	EVMJF538 for TCXO omit the V	Package Size '538': 5 x 3.2mm		P: LVPECL D: LVDS C: HCSL Q: CML		156.250 (MHz)

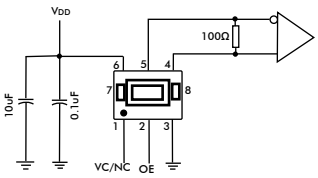
TEST CIRCUITS

LVPECL

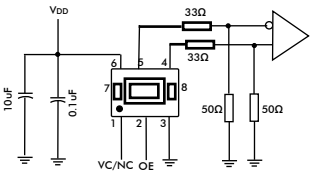


VDD= 3.3V: R1=R3=127Ω ; R2=R4= 82.5Ω
VDD= 2.5V: R1=R3= 250Ω ; R2=R4= 62.5Ω

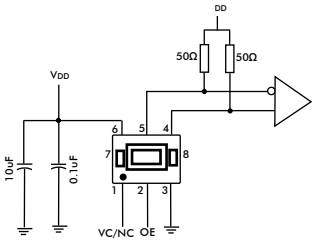
LVDS



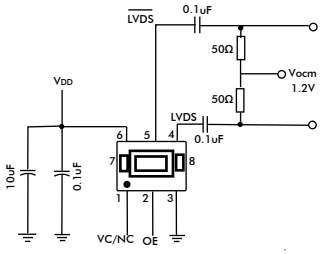
HCSL



CML



LVDS 1.8V only



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