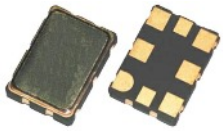
EUROQUARTZ EG_JF SERIES CRYSTAL VCXO OSCILLATORS

High Frequency - Ultra-Low Jitter 15MHz to 2100MHz

FEATURES

- **EG_JF Series oscillators, Ultra-low Jitter**
- **Outputs CMOS, LVPECL, LVDS, CML Differential outputs: 15~2100MHz**
- **HCSL Differential Outputs: 15~700MHz**
- **RMS phase jitter 150fs ftypical**
- **ITAR Free**



GENERAL SPECIFICTIONS

Model	EGTJF	EGPJF	EGDJF	EGQJF	EGCJF
Output Logic Type	**CMOS**	**LVPECL**	**LVDS**	**CML**	**HCSL**
Frequency Range	15 ~250MHz	15 ~ 2100MHz	15 ~ 2100MHz	15 ~ 2100MHz	15 ~ 700MHz
Load	15pF max	50Ω into VDD-2V or Thevenin equivalent	100Ω between OUT and OUT-1	50Ω to VDD	50Ω to GND
Power Supply Voltage (VDD)	+1.8V±5% or +2.5V±10% or +3.3V±10%	+2.5V±10% or +3.3V±10%	+1.8V±5% +2.5V±10% +3.3V±10%	+1.8V±5% +2.5V±10% +3.3V±10%	+1.8V±5% or +2.5V±10% or +3.3V±10%
Output 'HIGH' Voltage	VDD -0.4V min	VDD-1.165V min. VDD-0.8V max.	VDD: 1.4V typical VDD: 1.6V max.	VDD: -0.085V min. VDD: = max.	VDD: 0.66V min. VDD: 1.15V max.
Output 'LOW' Voltage	VDDx 0.1 max 0.3V max for 1.8V	VDD: -2.0V min.	VDD: 1.1V typical	VDD: -0.6V min.	VDD: 0.0V min.
Duty Cycle	50%±5% 50%±10% 1.8V only	50%±5%	50%±5%	50%±5%	50%±5%
Rise Time (Tr) Fall Time (Tf) (20% ~ 80% waveform)	5.0ns max.	0.4ns max.	0.4ns max.	0.4ns max.	0.4ns max.
Current Cons. 50MHz: at VDD = 3.3V 250MHz:	70mA typical 80mA typical	100mA typical 120mA max.	75mA typical 90mA max.	70mA typical 85mA max.	80mA typical 100mA max.
Current with output Disabled	63mA typical	99mA typical	74mA typical	69mA typical	79mA typical
RMS Phase Jitter (Typical) 12kHz to 20MHz	156.250MHz: 159fs ; 491.520MHz : 155fs ; 644.530 MHz : 151fs ; 2000MHz : 163fs				
Output Voltage Swing	---------	595mV(min) 930mV (max)	250mV (min) 450mV (max)	200mV (min) 600mV (max)	620mV (min) 780mV (max)
Storage Temp	-55C +150C max limits				
Ageing at Ta = 25°C	±3ppm max. first year; 2±ppm max. per year thereafter				
V Cont Centre	+0.9V for VDD = +1.8V	+1.25V for VDD = +2.5V	+1.65V for VDD = +3.3V		
V Cont Range	+0.0V ~ +1.8V	+0.25 ~ +2.25V	+0.3V ~ +3.0V		
Freq Pulling Range	±100ppm min. ±200ppm available	±100ppm min. ±200ppm availablle	±100ppm min. ±200ppm available		
Linearity	±1% typical ; ±10% max				
V Cont I/P Impedance	5 MΩ (min)				
Bandwidth	10kHz typ. Measure at -3dB				

Frequency Stability Codes	Frequency stability over operating temp. Range	±25ppm	±50ppm	±100ppm	If non-standard please enter the desired stability after the 'C' or 'I' Example: 'C20' is ±20ppm over -10° to +70°C.
	Commercial -10° to +70°C	A	B	C	
	Industrial -40° to 85°C	D	E	F	

EUROQUARTZ LIMITED Blacknell Lane CREWKERNE Somerset UK TA18 7HE
Tel: +44 (0)1460 230000 info@euroquartz.co.uk www.euroquartz.co.uk

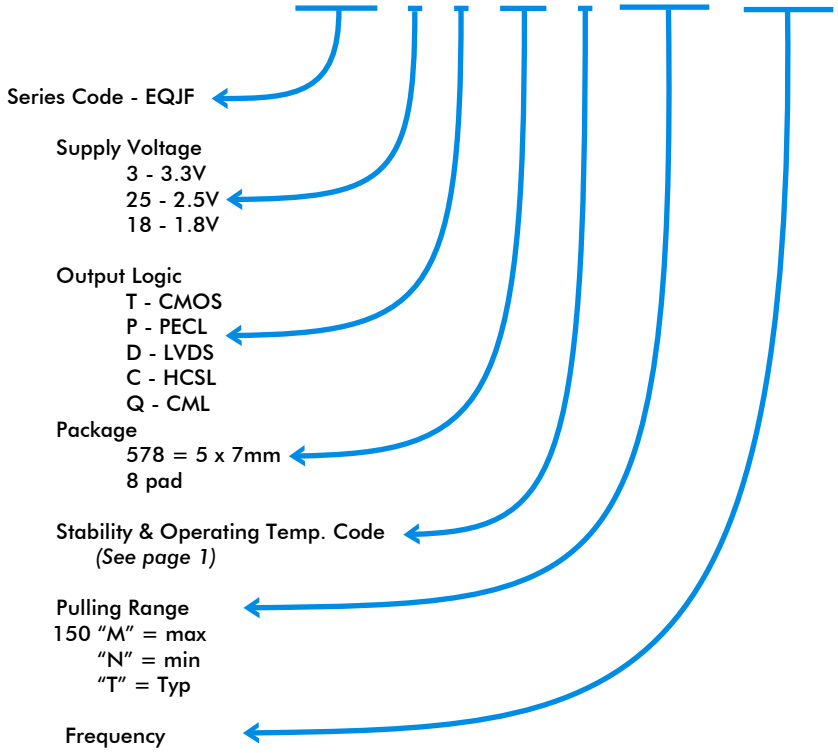
ENVIRONMENTAL PERFORMANCE SPECIFICATION

Green Requirement	ROHS Compliant, pB (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)
Second Level Interconnect	e4
Moisture Sensetivity Level	Level 1 (infinite) according to IPC/JEDEC J-STD-020D.1
Storage Temperature Range	-55° to +150°C
Humidity	85% RH, 85°C, 48 hours
Fine Leak	MIL-STD-883 Method 1014, condition A
Gross Leak	MIL-STD-883 Method 1014, condition C
Solderability	MIL-STD-202F Method 208E
Reflow	260°C for 10 seconds, twice
Vibration	MIL-STD-202F Method 204, 35G, 50 to 2000Hz
Shock	MIL-STD-202F Method 213B, test cond. E, 1000g ½ sine wave
Resistance to Solvent	MIL-STD-202F Method 215
Temperature Cycling	MIL-STD-883 Method 1010
ESD Rating	Human body model (HBM): 2000V min.
Pad Surface Finish	Gold (0.3µm to 1.0µm) over nickel (1.27µm to 8.89µm)
Weight of Device	0.045 gm typical

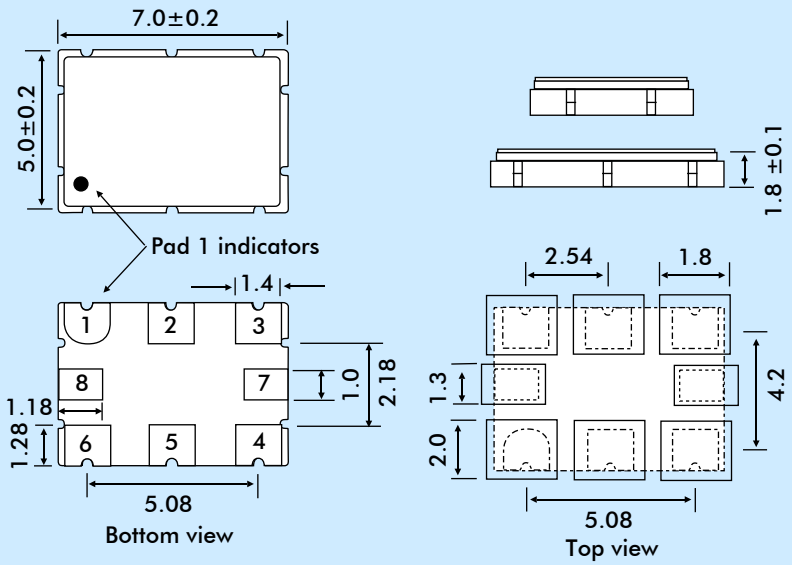
PART NUMBERING

EQJF oscillator part numbers are configured as per the following example: EG_JF-3-P-578-E-150M-250MHz

EG_JF - 3 - P - 578 - E - 150M - 250MHz

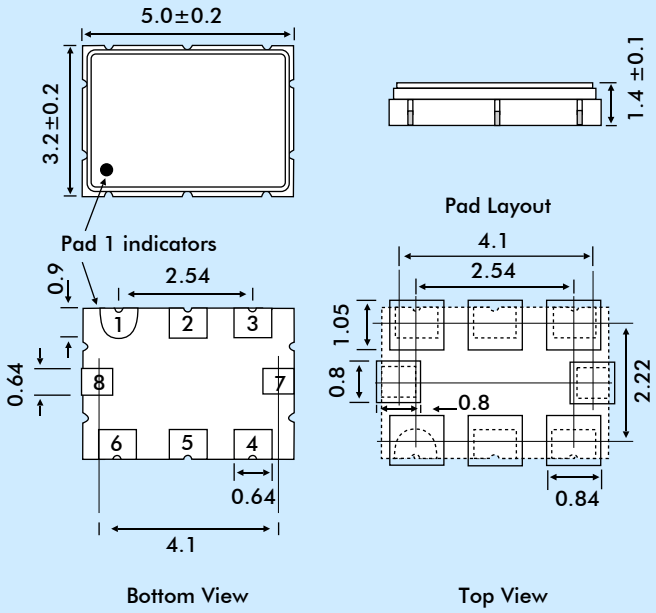


OUTLINE & DIMENSIONS



Pad Connections

1 Voltage Control
2 Output Enable
3 Ground
4 Output
5 Complimentary Output - Not Connected if CMOS
6 Supply Voltage
7 Do not connect
8 Do not connect



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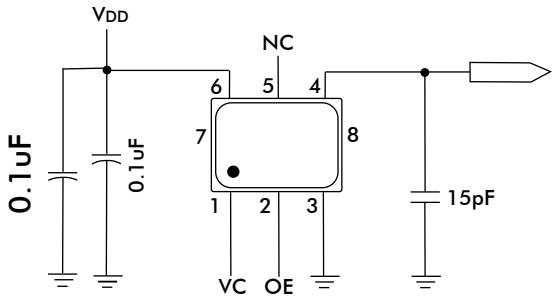
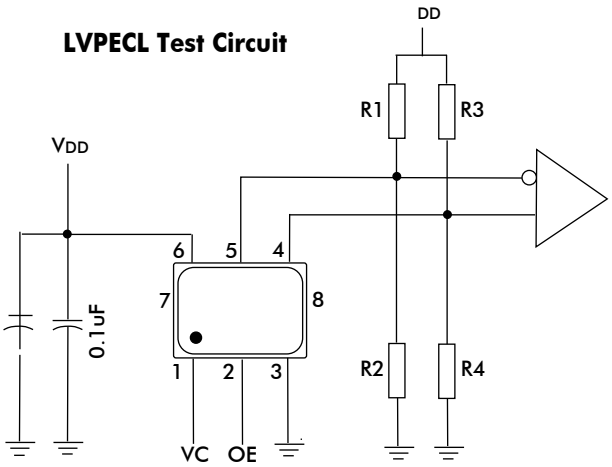
CMOS Test Circuit

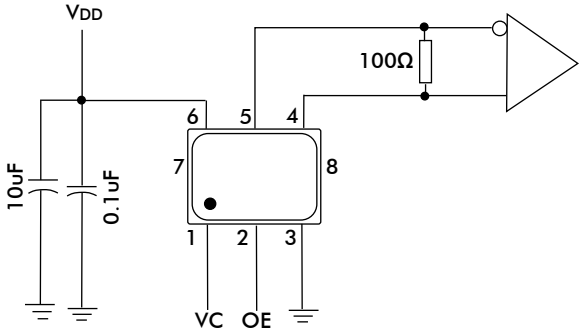


LVPECL Test Circuit

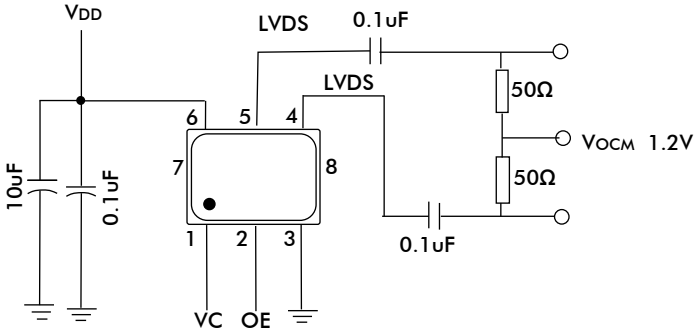


VDD = 3.3v ; R1=R3=127Ω ; R2-R4=82.5Ω
VDD = 2.5v ; R1=R3=250Ω ; R2-R4=62.5Ω

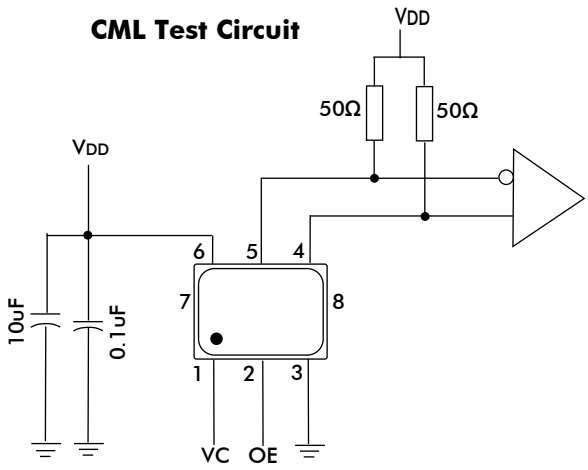
LVDS Test Circuit (3.3V and 2.5V)



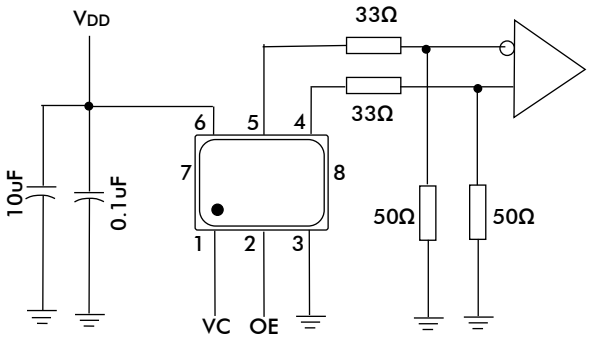
LVDS Test Circuit (1.8V only)



CML Test Circuit



HCSL Test Circuit



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