## Introduction

As more advances are made in the processor, multi-media and networking technologies, they demand more bandwidth than ever before. Point-to-point physical interfaces are starting to become obsolete, as they struggle to keep up with the increasing data rates. In order to get around the physical limitations, common mode logic has been utilized in order to provide high speed, low power interface standards.

This technical note sets out to explain and differentiate between the main logic interfaces available today: LVPECL; LVDS; HCSL; CML.

**Why Differential Signalling?**

One of the biggest problems in RF circuits is the possibility of the input wave being distorted by EMI during transmission, resulting in a noisy signal.

When a signal is transmitted through a single-ended connection, any noise imposed on it during transmission affects output, which might give an unreliable, distorted wave.

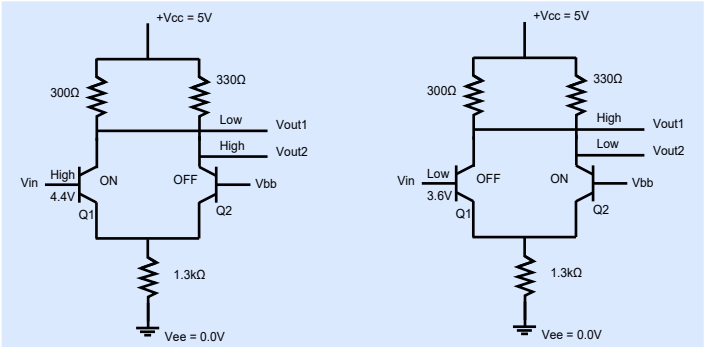
In differential signalling, two wires are often twisted together becoming EMI coupled, meaning that the interference they experience is more or less the same, making the voltage difference between the wires almost 0V. This allows one of the wires to act as a reference of what the signal is supposed to look like, making the output come out as intended.

Differential signals are overall more noise immune than their single-ended counterparts.

## LVPECL

Low Voltage Positive Emitter-Coupled Logic (LVPECL) originally started out as Emitter-Coupled Logic (ECL).

ECL was one of the earlier technologies that allowed for fast switching speed, as well as having a propagation time comparable to CMOS.




**ECL Circuit**

The circuit pictured above shows the operation of the ECL interface.

When a 'high' input enters the circuit through Vin, Q1 is turned on, and Q2 is turned off. During this, Q1 is not saturated, which puts Vout2 to high, and Vout1 to low, because of the drop within the 300Ω. This behaviour is mirrored when a 'low' input enters the circuit through Vin. Q1 will turn off, Q2 will turn on, and due to the drop in voltage on the 330Ω resistor, Vout1 will be high and Vout2 will be low.

The input high and low voltages are defined by the supply voltage, base voltage and voltage-at-emitter values. In this example, Vcc = 5V, Vbb = 4V and Vee = 0V. This makes the input values for high and low to be 4.4V and 3.6V respectively.

While, ECL has been one of the most popular interfaces that is still used in some applications, it has it's drawbacks; low noise margin, high power dissipation, level shifters are needed to interface with other logic gates, and most importantly, it runs off of the negative power rail. This is problematic, as it makes it difficult to interface with other logic families, as they ground the negative rail. The negative power supply was originally used as it minimized the effect of power supply variations on the logic levels of the gates.

This lead to the rise of Positive Emitter-Coupled Logic (PECL), which in-turn lead to the creation of Low Voltage Positive Emitter-Coupled Logic (LVPECL)

**Are there any differences between ECL, PECL, and LVPECL?**

PECL and LVPECL use positive supply voltage, whereas ECL uses a negative power supply. That is the only major difference, however, and all three of these interfaces work in the same way.

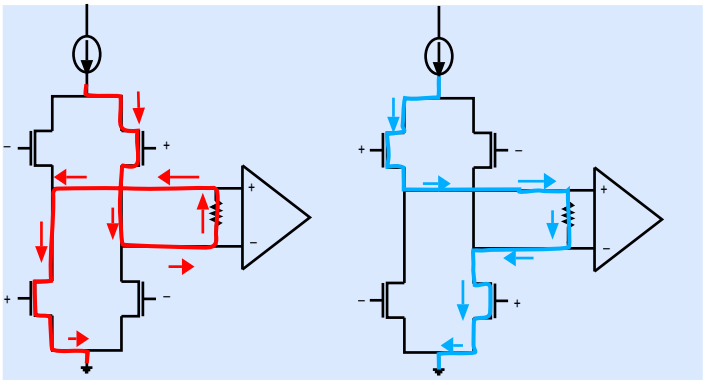
PECL allowed for the use of a 5V positive supply, which eased the design of circuits, as well as minor power savings.

LVPECL is now the most commonly used ECL interface, as it maintains the fast switching speed and low propagation time of the ECL, while cutting down on supply voltage by about 50%.

## LVDS

Low Voltage Differential Signalling (LVDS) uses differential transmission, which has a massive advantage over single-ended schemes, as it makes it less susceptible to common mode noise. Any noise coupled onto the interconnect is seen as common mode modulation by the receivers, and is rejected, meaning that the receivers only respond to differential voltage. LVDS was primarily designed for point-to-point applications, however Bus LVDS (BLVDS) is defines to support multi-point applications.

Unlike the ECL family, LVDS is not dependent on a specific supply voltage. This allows it to be used as a safe bet when taking the longevity of a circuit's design into consideration, as it allows easy migration from 5V to 3.3V or 2.5V, while still maintaining it's performance.



**LVDS Circuit and Current Flow**

LVDS is different from other logic interfaces, as instead of using voltage swings, it utilizes current swings instead. It operates by controlling the polarity of current flowing through the circuit.

The current flows through the resistor that matches the line impedance (usually 100Ω) to avoid reflections at high frequencies. When passing through the resistor, a voltage drop is crated at the receiver inputs. The receiver subtracts the two voltages to obtain a differential value. If a 3.5mA current was injected into the circuit, and it passes through a 100Ω resistor, it will generate a voltage of 350mV (according to Ohm's law). The receiver is able to sense the polarity of the current passing through it to determine the logic level.

The LVDS transmitter consumes a constant current, which puts a lot less demand on power supply decoupling, which produces less interference in power and ground levels of the circuit.

The advantages of using LVDS is the improvement of electromagnetic compatibility, combined with low voltage operation. The voltage compliance is also doubled, as the signal is not limited to single ended outputs.

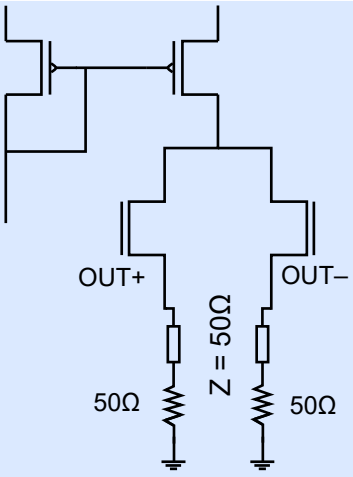
While LVDS has it's benefits, it's jitter performance is not as good as PECL, it's more expensive, and is limited in the maximum amount of supported data rate.

The most common use of LVDS is transferring data from a processing unit to a display. This mainly includes transferring data to a LCD screen at 60Hz refresh rate. It was previously used in computers for data transfer from the motherboard to a display. Although AMD and Intel have stopped supporting LVDS since 2013, it is still commonly used in TVs and laptops.

## HCSL

High Speed Current Steering Logic (HCSL) is the most popular and supported logic interface used for PCIe applications, as well as Intel chipsets.

HCSL produces a very minimal amount of noise while operating at low currents (94mA typically, 115mA max.). lying between LVDS and LVPECL interfaces. This is why it is chosen for motherboard operations, as it is able to produce clear, noise free signals.

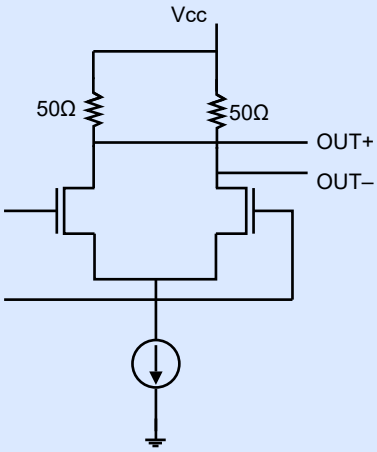



**HCSL Circuit**

HCSL operates by passing a signal through a differentiator, which produces a positive wave, as well as a negative counterpart to it. These two waves, then go into a substractor, that is terminated by resistors. The substractor amplifies the positive portion of the signal, resulting in an output that has double the amplitude of the original signal.

## CML

Common Mode Logic (CML) is one of the simplest high speed logic interfaces. It provides a low output voltage swing, which results in low power consumption.




**CML Circuit**

CML operates on the principle of current steering. The current is steered between two alternate paths. Depending on the path the current is sent down, it results in a '1' or '0' being represented at the output.

CML is most commonly used in fibre optic components, as it produces very little noise with the correct termination, as well as being able to transmit a lot of data (~312.5Mbit/s to 3.125Gbit/s) on printed circuit boards.
The main advantage of CML over the ECL family, is that it uses 50Ω termination, whereas ECL has a very low resistance at the output. The 50Ω termination prevents any reflections and noise from endind up in the output waveform. CML also has the advantage of using very little power, having a voltage swing of around 400mV, which is half of LVPECL and only a little higher than LVDS. CML is also compatible with 1.8V, 2.5V, 3.3V and 5.0V supply voltages.