

8 pin Dual-in-Line VCXO

- Frequency range 38MHz to 640MHz
- LVDS Output
- Supply Voltage 3.3 VDC
- Phase jitter 0.4ps typical
- Pull range from ± 30 ppm to ± 150 ppm



DESCRIPTION

GDW8VCXOs are packaged in an industry-standard, 8pin dual-in-line package. Typical phase jitter for GDW series VCXOs is 2.35ps. Output is LVDS. Applications include phase lock loop, SONET/ATM, set-top boxes, MPEG, audio/video modulation, video game consoles and HDTV.

SPECIFICATION

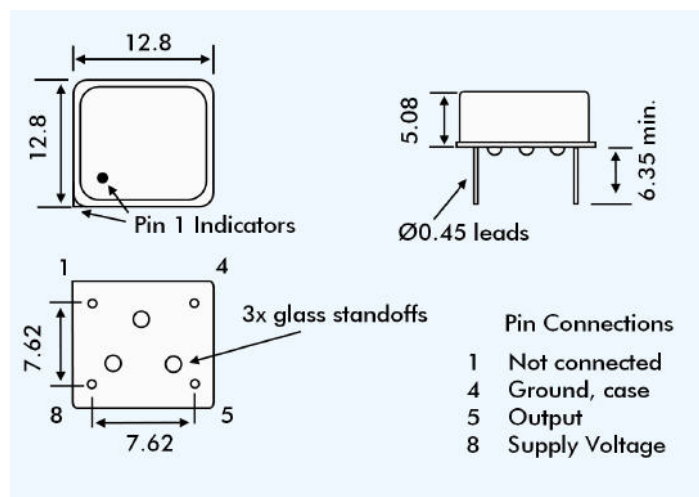
Frequency Range:	750kHz to 800.0MHz
Supply Voltage:	3.3 VDC $\pm 5\%$
Output Logic:	LVDS
RMS Period Jitter:	4.3ps typical
Peak to Peak Jitter:	27.0ps typical
Phase Jitter:	2.35ps typical
Initial Frequency Accuracy:	Tune to the nominal frequency with $V_c = 1.65 \pm 0.2$ VDC
Output Voltage HIGH (1):	1.4 Volts typical
Output Voltage LOW (0):	1.1 Volts typical
Pulling Range:	From ± 30 ppm to ± 150 ppm
Control Voltage Range:	1.65 ± 1.35 Volts
Temperature Stability:	See table
Output Load:	50Ω into Vdd or Thevenin equiv.
Rise/Fall Times:	0.5ns typ., 0.7ns max. 20% Vdd to 80% Vdd
Duty Cycle:	50% $\pm 5\%$ (Measured at Vdd-1.3V)
Start-up Time:	10ms maximum, 5ms typical
Current Consumption:	55mA typical, 60mA maximum (At 202.50MHz)
Static Discharge Protection:	2kV maximum
Storage Temperature:	-55° to $+150^\circ$ C
Ageing:	± 2 ppm per year maximum
Enable/Disable:	Not implemented - 4 pin package
RoHS Status:	Fully compliant or non compliant

FREQUENCY STABILITY

Stability Code	Stability \pm ppm	Temp. Range
A	25	$0^\circ \sim +70^\circ$ C
B	50	$0^\circ \sim +70^\circ$ C
C	100	$0^\circ \sim +70^\circ$ C
D	25	$-40^\circ \sim +85^\circ$ C
E	50	$-40^\circ \sim +85^\circ$ C
F	100	$-40^\circ \sim +85^\circ$ C

If non-standard frequency stability is required
Use 'I' followed by stability, i.e. I20 for ± 20 ppm

OUTLINE & DIMENSIONS



PART NUMBERING

