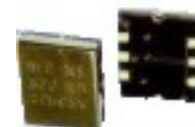


- Frequency range 750kHz to 800MHz
- LVPECL Output
- Supply Voltage 3.3 VDC
- Phase jitter 2.35ps typical
- Pull range from ± 30 ppm to ± 150 ppm



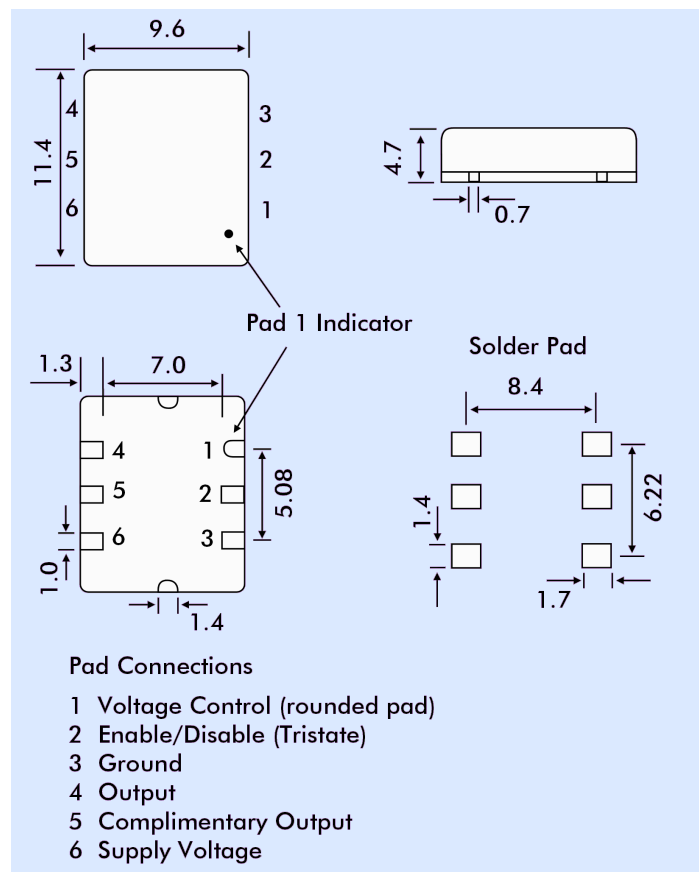
DESCRIPTION

GPW64 VCXOs are packaged in a 6 pad 7mm x 5mm SMD package. Typical phase jitter for GPW series VCXOs is 2.35ps. Output is LVPECL. Applications include phase lock loop, SONET/ATM, set-top boxes, MPEG, audio/video modulation, video game consoles and HDTV.

SPECIFICATION

Frequency Range:	750.0kHz to 800.0MHz
Supply Voltage:	3.3 VDC $\pm 5\%$
Output Logic:	LVPECL
RMS Period Jitter:	4.3ps typical
Peak to Peak Jitter:	27.0ps typical
Phase Jitter:	2.35ps typical
Initial Frequency Accuracy:	Tune to the nominal frequency with $V_c = 1.65 \pm 0.2$ VDC
Output Voltage HIGH (1):	Vdd-1.025V minimum Vdd-0.880V maximum
Output Voltage LOW (0):	Vdd-1.810V minimum Vdd-1.620V maximum ($R_L = 50\Omega$ to Vdd-2V)
Pulling Range:	From ± 30 ppm to ± 150 ppm
Control Voltage Range:	1.65 ± 0.35 Volts
Temperature Stability:	See table
Output Load:	50 Ω into Vdd or Thevenin equiv.
Rise/Fall Times:	0.5ns typ., 0.7ns max. 20% Vdd to 80% Vdd
Duty Cycle:	50% $\pm 5\%$ (Measured at Vdd-1.3V)
Start-up Time:	10ms maximum, 5ms typical
Current Consumption:	75mA maximum at 212.5MHz 80mA maximum at 622.08MHz
Static Discharge Protection:	2kV maximum
Storage Temperature:	-55 $^{\circ}$ to +150 $^{\circ}$ C
Ageing:	± 2 ppm per year maximum
Enable/Disable:	See table
RoHS Status:	Fully compliant or non-compliant versions available

OUTLINE & DIMENSIONS



FREQUENCY STABILITY

Stability Code	Stability \pm ppm	Temp. Range
A	25	0 $^{\circ}$ ~+70 $^{\circ}$ C
B	50	0 $^{\circ}$ ~+70 $^{\circ}$ C
C	100	0 $^{\circ}$ ~+70 $^{\circ}$ C
D	25	-40 $^{\circ}$ ~+85 $^{\circ}$ C
E	50	-40 $^{\circ}$ ~+85 $^{\circ}$ C
F	100	-40 $^{\circ}$ ~+85 $^{\circ}$ C

If non-standard frequency stability is required Use 'I' followed by stability, i.e. I20 for ± 20 ppm

ENABLE/DISABLE FUNCTION

Tristate Pad Status	Output Status
Not connected Below 0.3Vdd (Ref. to ground)	LVPECL and Complimentary LVPECL enabled Both outputs are disabled (high impedance)
Above 0.7Vdd (Ref. to ground)	Both outputs are enabled

PART NUMBERING

